

**REMARKS**

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1, 2, 7, 8, 13 and 15-18 are pending in the present application. Claims 1, 2, 8, 13 and 15-18 stand rejected. Claim 7 was allowed. The rejections set forth in the Office Action are respectfully traversed below.

**Claim Rejections – 35 U.S.C. §102**

Claims 1-2, 8, 13 and 15-18 were rejected under 35 U.S.C. §102(b) as being anticipated by **Freeman** (RE 34,363, previously cited). For the reasons set forth in detail below, this rejection, to the extent it is considered to apply to the presently amended claims, is respectfully traversed.

Independent claims 1, 2, 13 and 15-17 have been amended by the present Amendment to clarify that the claimed second inversion section (or second inverter) inverts an input signal having a logic level that is always opposite to the logic level of the signal input to the first inversion section. Support for this change is provided, e.g., in Fig. 1 of the drawings, which illustrates a first input signal A and a second input signal XA (i.e., the inverted signal of A).

Further, each of independent claims 1, 2, 13 and 15-17 have been amended to clarify that the transmission section (or outputting section, or selector outputs one of the inverted first input signal and the inverted second input signal in response to *only* an externally controllable selection signal and an inverted signal of the selection. Support for this change is provided, e.g.,

in Fig. 1 of the drawings, which illustrate selection signal S and an inverted signal of the selection signal XS.

First, **Freeman** does not disclose or suggest that the inputs A, B to the inverters 21, 22, respectively, are *always* opposite logic levels. To the contrary, **Freeman** indicates that A and B are variables (see column 3, line 11), which indicates that A, B would take on any of the values 00, 01, 10 and 11. Thus, the variables A, B are not *always* opposite logic levels.

Second, **Freeman** does not disclose or suggest a transmission section (or outputting section, or selector) that outputs one of an inverted first input signal and an inverted second input signal in response to *only* an externally controllable selection signal and an inverted signal of the selection signal. Unlike the claimed invention, the **Freeman** circuit shown in Fig. 2 requires more than two signals to select which output of the inverters 21, 22 is output. For example, **Freeman** requires four control signals to select whether \A and/or \B is output to the OR gate 23. That is, control signals C2 and \C2 are required to select whether \A is output to gate 23, while control signals C3 and \C3 are required to determine whether \B is output to gate 23. Thus, **Freeman** requires four control signals to select an output signal.

In view of the above amendments and remarks, it is respectfully submitted that each of claims 1, 2, 13 and 15-17 patentably distinguish over the cited prior art and therefore define allowable subject matter.

Claim 8

On page 7, Item 6c of the Office Action, the Examiner responds to the patentability arguments regarding dependent claim 8. Applicants respectfully disagree with the Examiner's rejection of claim 8. More particularly, the Examiner asserts that the pass transistors associated with control signals C2 and /C2 "would pass the inverted signal otherwise it would block the inverted signal and pass the un-inverted signal." However, the pass transistors associated with control signals C2 and /C2 have nothing to do with whether the input signal A is passed *to* the inversion section 21. Instead, the pass transistor associated with control signal C2 controls whether the inverted signal is passed *from* the inversion section 21 and input to gate 23.

In other words, the pass transistors of the present invention control whether the input signal A is passed to the inversion section, whereas the pass transistors of **Freeman** control whether the inverted signal is passed from the inversion section 21 and input to gate 23. Therefore, **Freeman** fails to disclose or suggest the features of claim 8. Further, in the absence of considerable reconstruction of the **Freeman** reference, one of ordinary skill in the art would not reach the subject matter recited in claim 8.

Accordingly, for the reasons set forth above, reconsideration and withdrawal of the rejection of claim 8 are respectfully requested.

Application No. 09/522,470  
Group Art Unit: 2193

Amendment under 37 C.F.R. §1.114  
Attorney Docket No.: 000267

**CONCLUSION**

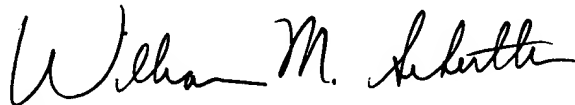
In view of the foregoing amendments and accompanying remarks, it is submitted that all pending claims are in condition for allowance. A prompt and favorable reconsideration of the rejection and an indication of allowability of all pending claims are earnestly solicited.

If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

**WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP**

A handwritten signature in black ink, appearing to read "William M. Schertler". The signature is fluid and cursive, with the first name "William" and last name "Schertler" being clearly legible, and "M." in the middle.

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